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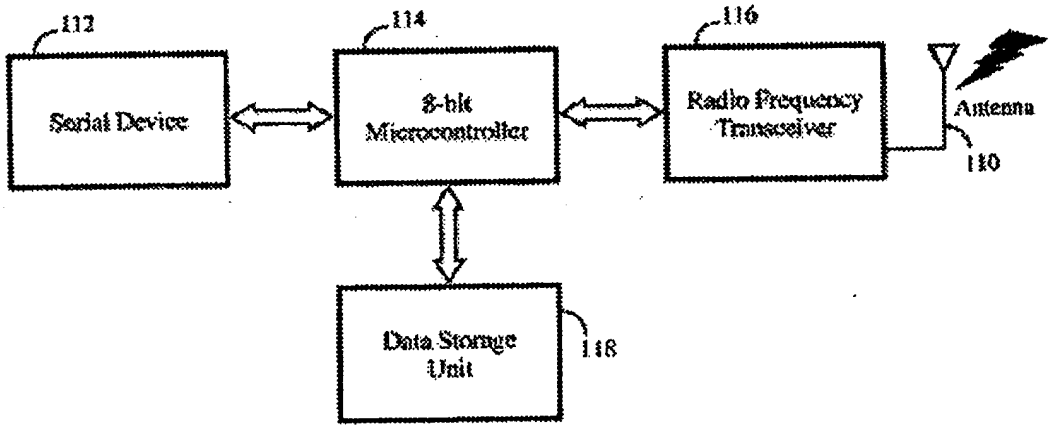

Fig 1
Single Node Hardware Architecture

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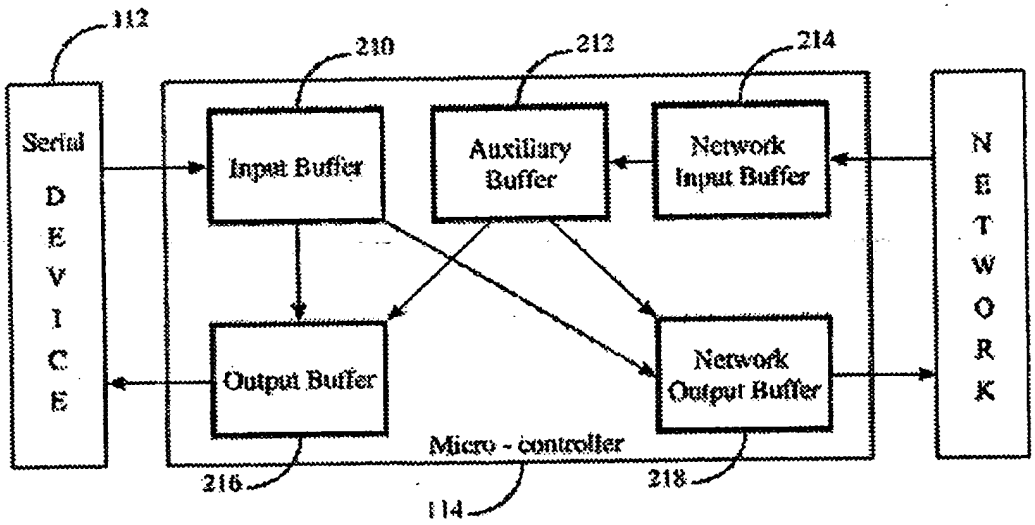

Fig 2
Data Flow In Microcontroller

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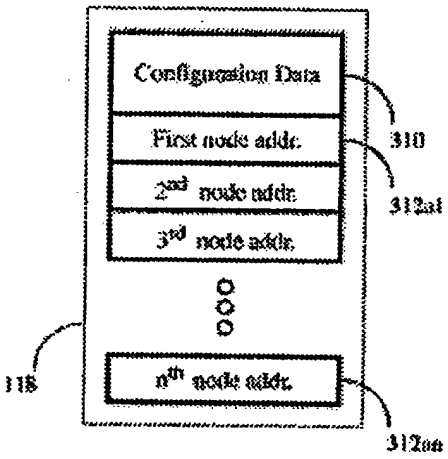

Fig 3
Architecture of Data Storage Unit

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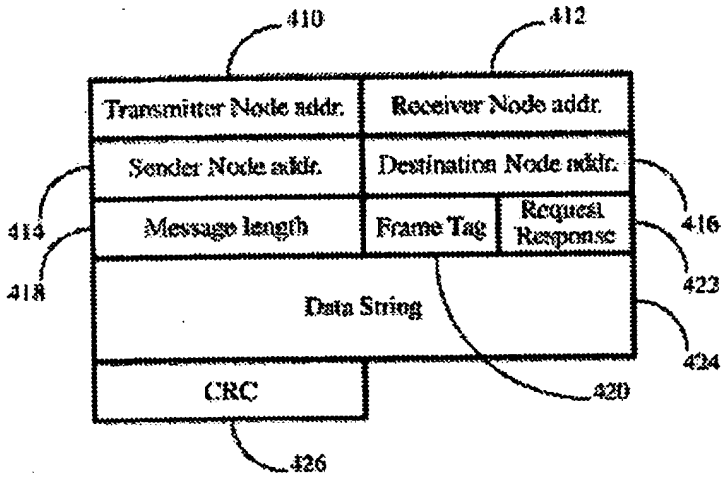

Fig 4
Header Fields

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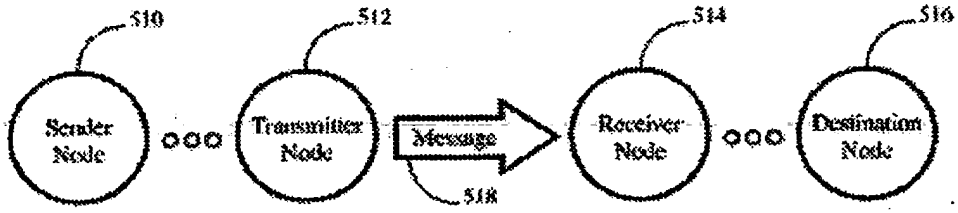

Fig 5
Message Transmission in a Multi-Hop Network

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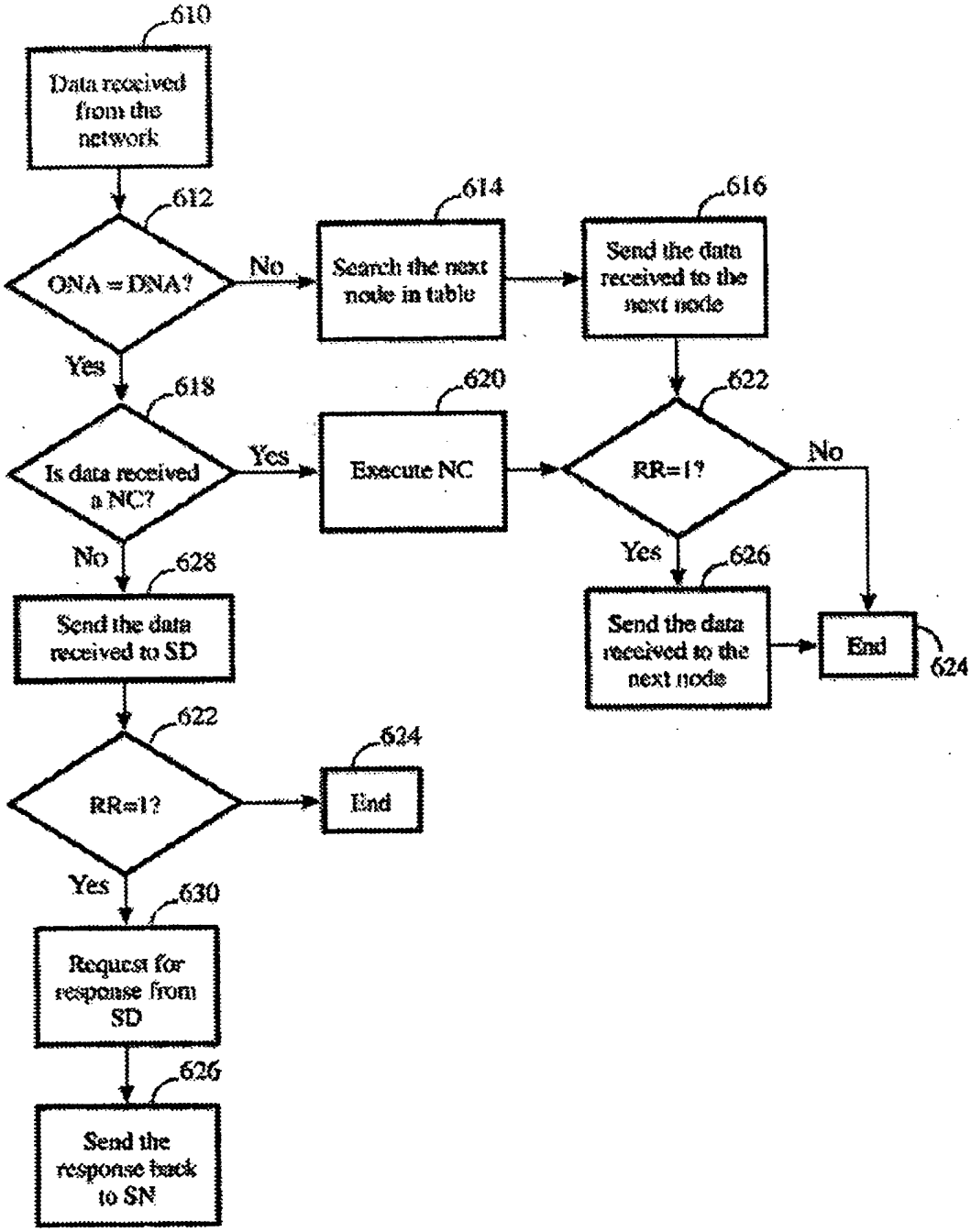

Fig 6
Request Response Algorithm